a semiconductor substrate;

a silicon oxide layer formed over a surface of said semiconductor substrate;

a gate electrode formed over a first portion of said silicon oxide layer; and

a side wall structure which includes nitrogen formed over a second portion of said silicon oxide layer and adjacent said gate electrode,

wherein a thickness of said second portion of said silicon oxide layer is greater than a thickness of said first portion of said silicon oxide layer.

2. (Amended) A semiconductor device as claimed in claim 1, wherein the thickness of said second portion of said silicon oxide layer is at least twice the thickness of said first portion of said silicon oxide layer.

3. (Amended) A semiconductor device as claimed in claim 1, wherein the thickness of said second portion of said silicon oxide layer is at least 50% greater than the thickness of said first portion of said silicon oxide layer.

4. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a gate oxide layer formed over said semiconductor substrate;

a gate electrode formed over a first portion of said gate oxide layer;

a side wall structure which includes nitrogen formed adjacent said gate electrode; and

a diffusion deterrent layer formed between said side wall structure and said semiconductor substrate, wherein said diffusion deterrent layer prevents nitrogen in said side wall structure from diffusing into said semiconductor substrate,

wherein a thickness of said diffusion deterrent layer is greater than a thickness of said first portion of said gate oxide layer.

5. (Amended) A method for manufacturing a semiconductor device, comprising:

forming a gate oxide layer on a surface of a semiconductor substrate;

forming a gate electrode on a first portion of said gate oxide layer, said gate electrode having a cap layer formed thereon;

expanding a thickness of a second portion of said gate oxide layer other than said first portion of said gate oxide layer located under said gate electrode;

forming a side wall structure on the expanded second portion of said gate oxide layer and adjacent said gate electrode, said side wall structure including nitrogen;

forming an intermediate insulating layer over said cap layer and said side wall structure; and

forming a contact hole in said intermediate insulating layer using a Self Aligned Contact process.

6. (Amended) A method for manufacturing a semiconductor device as claimed in claim 5, wherein the thickness of said second portion of said gate oxide layer is at least twice a thickness of said first portion of said gate oxide layer.

7. (Amended) A method for manufacturing a semiconductor device as claimed in claim 5, wherein the thickness of said second portion of said gate oxide layer is at least 50% greater than a thickness of said first portion of said gate oxide layer.

8. (Amended) A method for manufacturing a semiconductor device as claimed in claim 5, wherein the thickness of said second portion of said gate oxide layer is expanded using CVD.

9. (Amended) A method for manufacturing a semiconductor device as claimed in claim 6, wherein the thickness of said second portion of said gate oxide layer is expanded using CVD.

10. (Amended) A method for manufacturing a semiconductor device as claimed in claim 7, wherein the thickness of said second portion of said gate oxide layer is expanded using CVD.

11. (Amended) A method for manufacturing a semiconductor device as claimed in claim 5, wherein the thickness of said second portion of said gate oxide layer is expanded using thermal oxidation.

12. (Amended) A method for manufacturing a semiconductor device as claimed in claim 6, wherein the thickness of said second portion of said gate oxide layer is

expanded using thermal oxidation.

13. (Amended) A method for manufacturing a semiconductor device as claimed in claim 7, wherein the thickness of said second portion of said gate oxide layer is expanded using thermal oxidation.

14. (Amended) A method for manufacturing a semiconductor device, comprising:

forming a gate oxide layer on a surface of a semiconductor substrate;

forming a gate electrode over a first portion of said gate oxide layer, said gate electrode having a cap layer formed thereon;

forming a side wall structure over a second portion of said gate oxide layer and adjacent said gate electrode, said side wall structure including nitrogen;

expanding a thickness of said second portion of said gate oxide layer located under said side wall structure using thermal oxidation, after said forming a side wall structure;

forming an intermediate insulating layer over said cap layer and said side wall structure; and

forming a contact hole in said intermediate insulating layer using a Self Aligned Contact process.

16. (Amended) A method for manufacturing a semiconductor device,

comprising:

forming a gate oxide layer on a surface of a semiconductor substrate;

forming a gate electrode over a first portion of said gate oxide layer, said gate oxide having a cap layer formed thereon;

forming a side wall structure on a second portion of said gate oxide layer and adjacent said gate electrode, said side wall structure including nitrogen;

forming an intermediate insulating layer over said cap layer and said side wall structure; and

forming a contact hole in said intermediate insulating layer using a Self Aligned Contact process,

wherein said side wall structure is formed by CVD at a temperature exceeding 850°C.

17. (Amended) A method for manufacturing a semiconductor device, comprising:

forming a gate oxide layer on a surface of a semiconductor substrate;

forming a gate electrode over a first portion of said gate oxide layer;

forming a cap layer over said gate electrode;

forming a first portion of a side wall structure over a second portion of said gate oxide layer and adjacent said gate electrode;

forming a second portion of said side wall structure on said first portion of said side wall structure over said second portion of said gate oxide layer and adjacent said

gate electrode;

forming an intermediate insulating layer over said cap layer and said side wall structure; and

forming a contact hole in said intermediate insulating layer using a Self Aligned Contact process,

wherein said first portion of said side wall structure is formed by CVD at a temperature exceeding 850°C.